HIGH-SPEED FULLY DIFFERENTIAL I/O AMPLIFIERS

FEATURES

- **High Performance**
  - **100 MHz, –3 dB Bandwidth**
  - **50 V/μs Slew Rate**
  - **75 dB Total Harmonic Distortion at 1 MHz (V_O = 2 V_{PP})**
  - **5.4 nV/√Hz Input-Referred Noise (10 kHz)**
- **Differential Input/Differential Output**
  - **Balanced Outputs Reject Common-Mode Noise**
  - **Differential Reduced Second Harmonic Distortion**
- **Power Supply Range**
  - **V_{DD} = 3.3 V**

DESCRIPTION

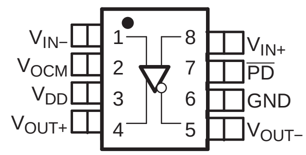
The THS412x is one in a family of fully differential-input, differential-output devices fabricated using Texas Instruments' state-of-the-art submicron CMOS process.

The THS412x consists of a true, fully differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion.

KEY APPLICATIONS

- **Simple Single-Ended To Differential Conversion**
- **Differential ADC Driver/Differential Antialiasing**
- **Differential Transmitter and Receiver**
- **Output Level Shifter**

THS4120
D, DGN, OR DGK PACKAGE
(TOP VIEW)



THS4121
D, DGN, OR DGK PACKAGE
(TOP VIEW)

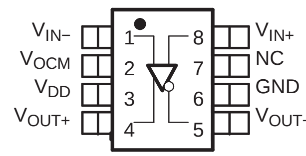


Table 1. HIGH-SPEED DIFFERENTIAL I/O FAMILY

DEVICE	NUMBER OF CHANNELS	POWERDOWN
THS4120 (1)	1	Yes
THS4121	1	–

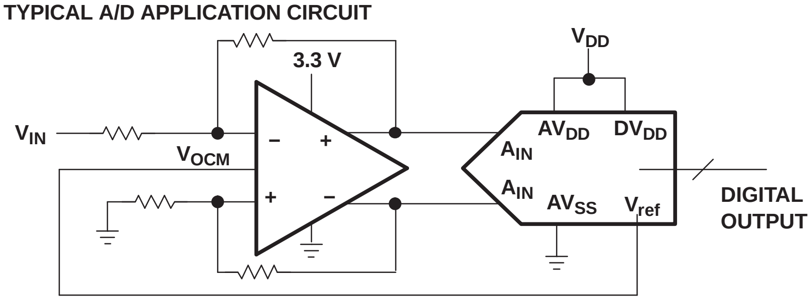
(1) For proper functiionality, an external 10-kΩ pullup resistor is required between the PD pin and the positive supply.

RELATED DEVICES

DEVICE (1)	DESCRIPTION	SINGLE SUPPLY VOLTAGE RANGE	SPLIT SUPPLY VOLTAGE RANGE
THS413x	150 MHz, 51 V/μs, 1.3 nV/√Hz	5 V to 30 V	±2.5 to ±15
THS414x	160 MHz, 450 V/μs, 6.5 nV/√Hz	5 V to 30 V	±2.5 to ±15
THS415x	150 MHz, 650 V/μs, 7.6 nV/√Hz	5 V to 30 V	±2.5 to ±15

(1) See the TI Web site for additional high-speed amplifier devices.

TYPICAL A/D APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES					EVALUATION MODULES
	SMALL OUTLINE(D)	MSOP PowerPAD™		MSOP		
		(DGN)	SYMBOL	(DGK)	SYMBOL	
0°C to 70°C	THS4120CD	THS4120CDGN	ARL	THS4120CDGK	ATZ	THS4120EVM
	THS4121CD	THS4121CDGN	ASB	THS4121CDGK	ATO	THS4121EVM
–40°C to 85°C	THS4120ID	THS4120IDGN	ARM	THS4120IDGK	ARN	–
	THS4121ID	THS4121IDGN	ASC	THS4121IDGK	ASN	–

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			UNIT
	Supply voltage, GND to V_{DD}		3.6 V
V_I	Input voltage		$\pm V_{DD}$
I_O	Output current (sink) (2)		110 mA
V_{ID}	Differential input voltage		$\pm V_{DD}$
	Continuous total power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature (3)		150°C
T_J	Maximum junction temperature, continuous operation, long-term reliability (4)		125°C
T_A	Operating free-air temperature	C suffix	0°C to 70°C
		I suffix	–40°C to 85°C
T_{stg}	Storage Temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds		300°C
	ESD ratings	HBM	4000 V
		CDM	1500 V
		MM	200 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS412x may incorporate a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPad™ thermally enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (1) (°C/W)	θ_{JC} (°C/W)	POWER RATING (2)	
			T_A = 25°C	T_A = 85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	260	54.2	385 mW	154 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	Split supply	±1.5	±1.65	±1.75	V
		Single supply	3	3.3	3.5	
T_A	Operating free-air temperature	C suffix	0		70	°C
		I suffix	–40		85	

ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB)	V_{DD} = 3.3 V,	Gain = 1, R_f = 200 Ω		100		MHz
SR	Slew rate(2)	V_{DD} = 3.3 V,	Gain = 1		55		V/µs
t_s	Settling time to 0.1%	Differential step voltage = 2 V_{PP}, Gain = 1			60		ns
	Settling time to 0.01%				292		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 200 Ω, R_L = 800 Ω, V_O = 2 V_{PP}	V_{DD} = 3.3 V,	f = 1 MHz		–75		dB
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 200 Ω, R_L = 800 Ω, V_O = 4 V_{PP}	V_{DD} = 3.3 V,	f = 1 MHz		–66		dB
	Spurious free dynamic range (SFDR) Differential input, differential output, V_O = 4 V_{PP}	R_f = 200 Ω,	f = 1 MHz		–69		dB
	Third intermodulation distortion	V_I = 0.071 V_{RMS}	Gain = 1, f = 10 MHz		–75		dBc
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			5.4		nV/√Hz
I_n	Input current noise	f = 10 kHz			1		fA/√Hz
DC PERFORMANCE							
	Open-loop gain	T_A = 25°C		60	66		dB
		T_A = full range			66		
V_S	Input offset voltage	T_A = 25°C			3	8	mV
		T_A = full range			4	9	
	Input offset voltage, referred to V_{OCM}	T_A = 25°C			5	13	
		T_A = full range				14	
	Offset voltage drift	T_A = full range			25		µV/°C
I_{IB}	Input bias current	T_A = full range			1.2		pA
I_{OS}	Input offset current				100		fA
	Current offset drift	T_A = full range			5		fA/°C

(1) The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.
(2) Slew rate is measured differentially from an output level range of 25% to 75%.

TEXAS INSTRUMENTS
www.ti.com

ELECTRICAL CHARACTERISTICS (Continued)

V_{DD} = 3.3 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)[(1)]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		64	96		dB
V_{ICR}	Common-mode input voltage range	T_A = full range		0.65 to V_{DD} – 0.1	0.35 to V_{DD}		V
r_i	Input resistance (dc level)	Measured into each input terminal			820		MΩ
C_i	Input capacitance, closed loop				3		pF
r_o	Output resistance	See Figure 16			1		Ω
OUTPUT CHARACTERISTICS							
V_{OH}	High-level output Voltage	$V_{IC} = V_{DD}/2$, V_{DD} = 3.3 V,	T_A = 25°C	3.05	3.15		V
V_{OL}	Low-level output Voltage	$V_{IC} = V_{DD}/2$, V_{DD} = 3.3 V,	T_A = 25°C	0.25	0.15		V
I_O	Output current (sink), R_L = 7 Ω	V_{DD} = 3.3 V,	T_A = 25°C	80	100		mA
I_O	Output current (source), R_L = 7 Ω	V_{DD} = 3.3 V,	T_A = 25°C	20	25		mA
POWER SUPPLY							
V_{DD}	Supply voltage range	Single supply			3.3		V
I_{DD}	Quiescent current (per amplifier)	V_{DD} = 3.3 V	T_A = 25°C		11	13.5	mA
			T_A = full range			16	
PSRR	Power-supply rejection ratio	T_A = 25°C		68	85		dB
POWER-DOWN CHARACTERISTICS (THS4120 ONLY)							
	Power-down voltage level[(2)]	Enable			>1.4		V
		Power down			<1.2		
	Power-down quiescent current	T_A = 25°C			120		µA
		T_A = full range			130		
t_{on}	Turn-on time delay	50% of final supply current value			4.8		µs
t_{off}	Turn-off time delay				3		ns
z_o	Output impedance	f = 1 MHz			1		kΩ

(1) The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.
(2) For detail information on the power-down circuit, see the power-down section in the application section of this data sheet.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Small-signal frequency response		1
SR	Slew rate		2
THD	Total harmonic distortion	vs Frequency	3
		vs Output voltage	4
	Harmonic distortion	vs Frequency	5, 6, 7
		vs Output voltage	8, 9
	Third intermodulation distortion	vs Output voltage	10
V_O	Output voltage	vs Load resistance	11
	Settling time		12
V_n	Voltage noise	vs Frequency	13
V_{OO}	Output offset voltage	vs Common-mode input voltage	14
CMMR	Common-mode rejection ratio	vs Frequency	15
z_{os}	Single-ended output impedance (closed loop)	vs Frequency	16

TYPICAL CHARACTERISTICS (continued)

			FIGURE
z_o	Single-ended (V_{OCM}) input impedance	vs Frequency	17

SMALL-SIGNAL FREQUENCY RESPONSE

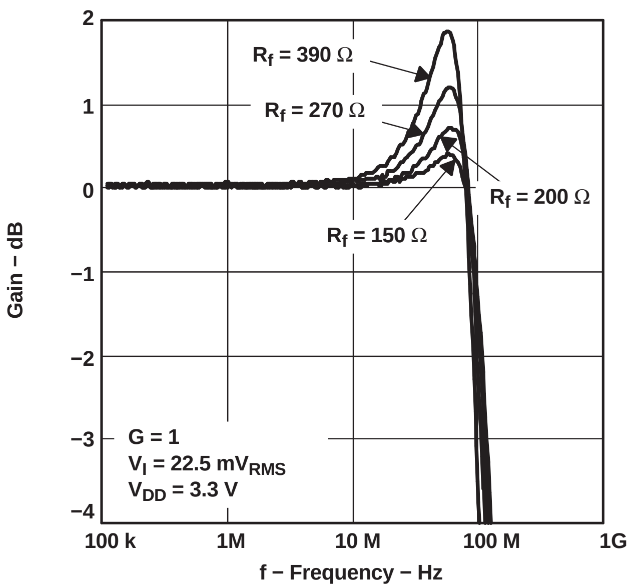


Figure 1.

SLEW RATE

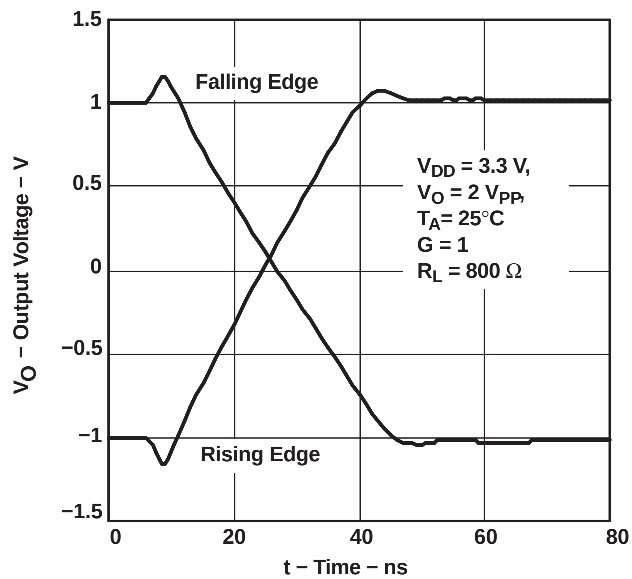


Figure 2.

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

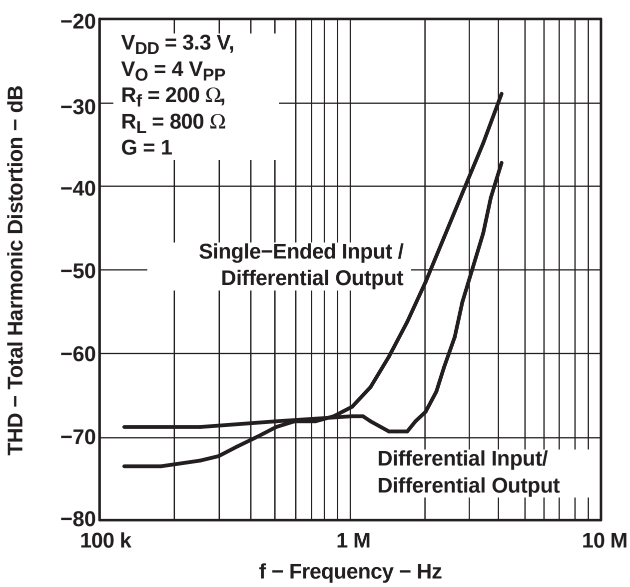


Figure 3.

TOTAL HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

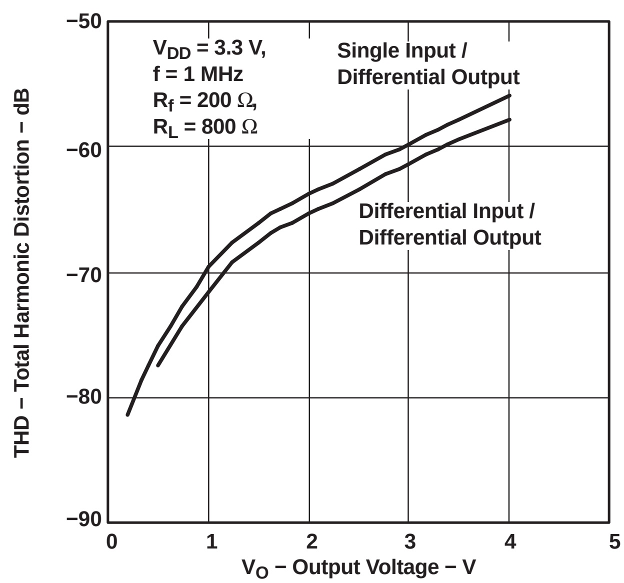


Figure 4.

THS4121
TOTAL HARMONIC DISTORTION
vs
FREQUENCY

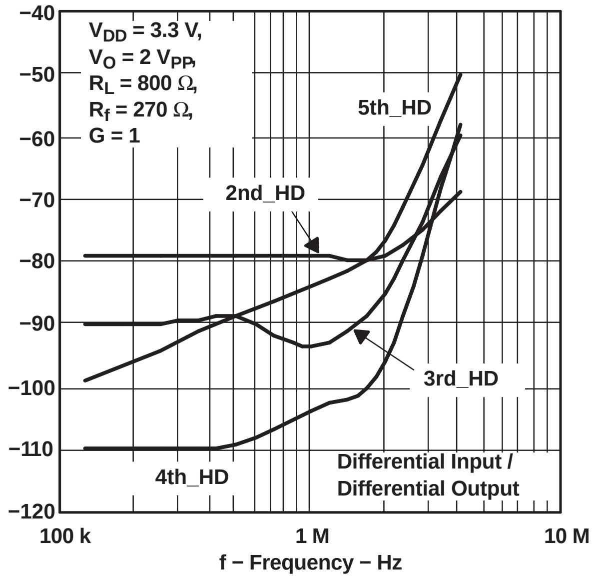


Figure 5.

THS4121
HARMONIC DISTORTION
vs
FREQUENCY

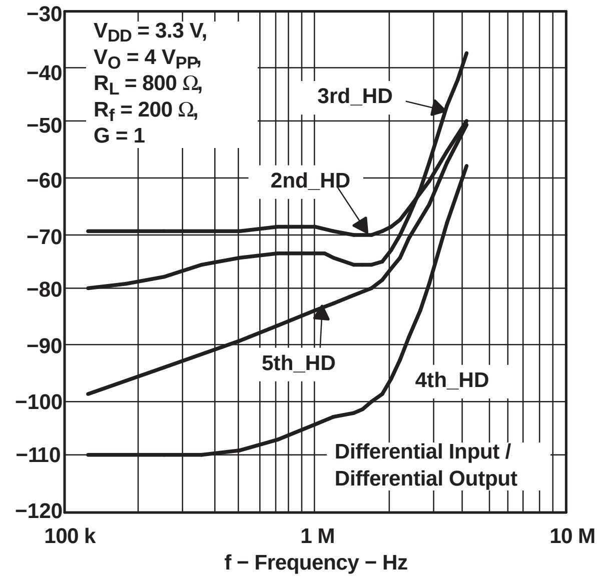


Figure 6.

THS4121
HARMONIC DISTORTION
vs
FREQUENCY

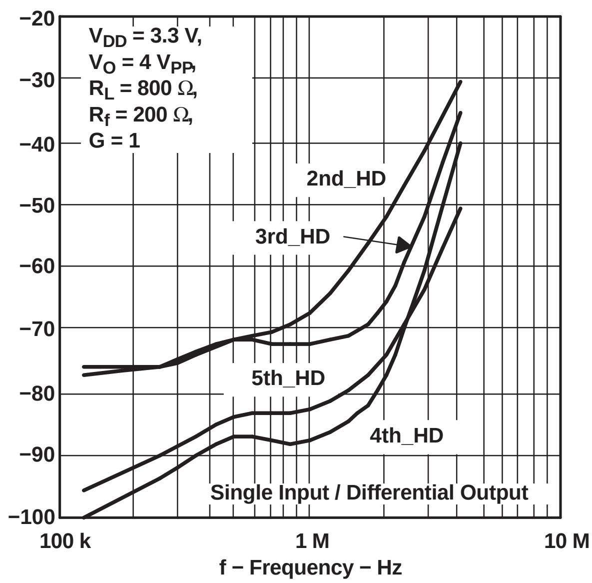


Figure 7.

THS4121
HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

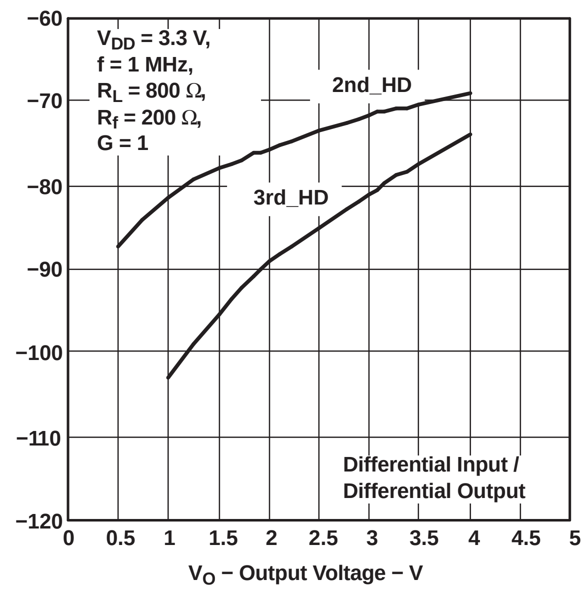


Figure 8.

THS4121
HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

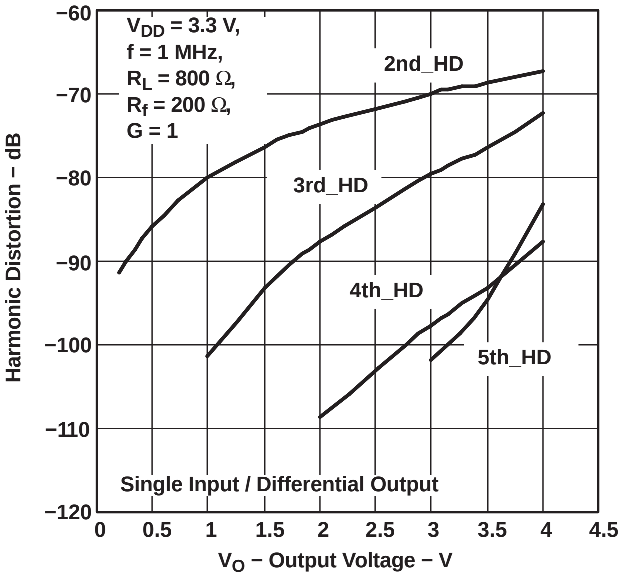


Figure 9.

THIRD INTERMODULALTION DISTORTION
vs
OUTPUT VOLTAGE

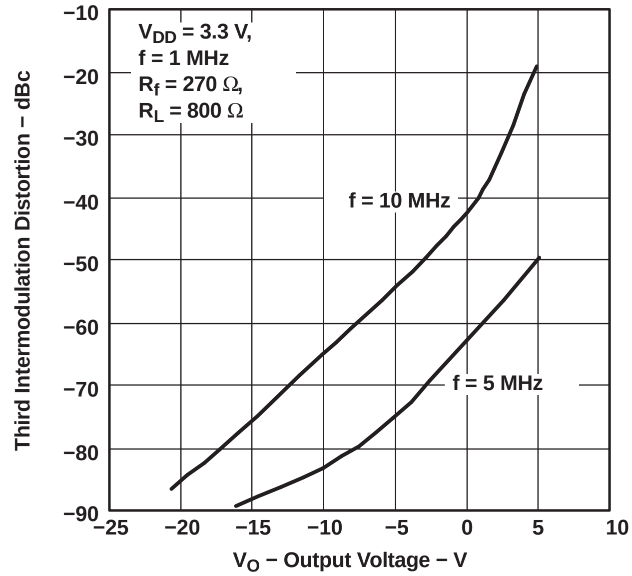


Figure 10.

THS4121
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

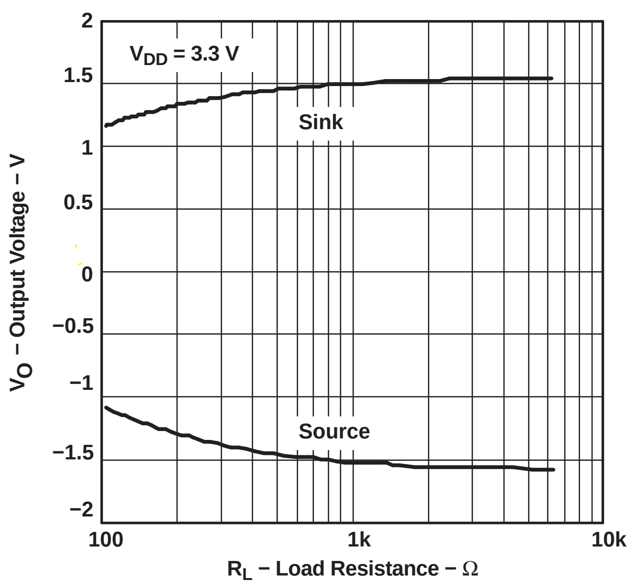


Figure 11.

SETTLING TIME

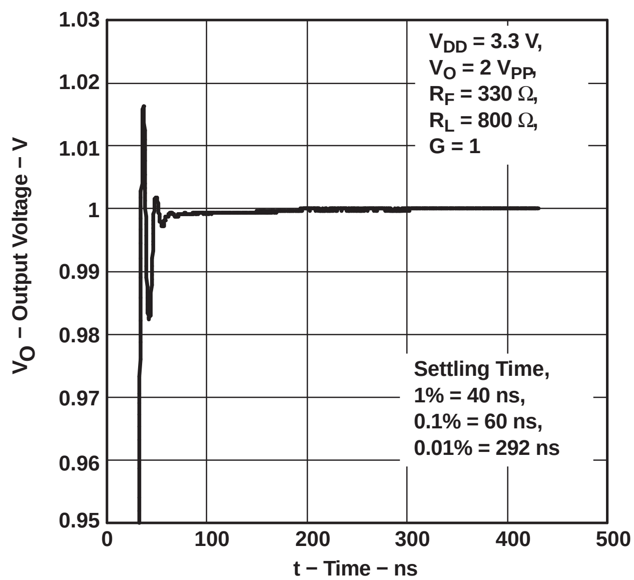


Figure 12.

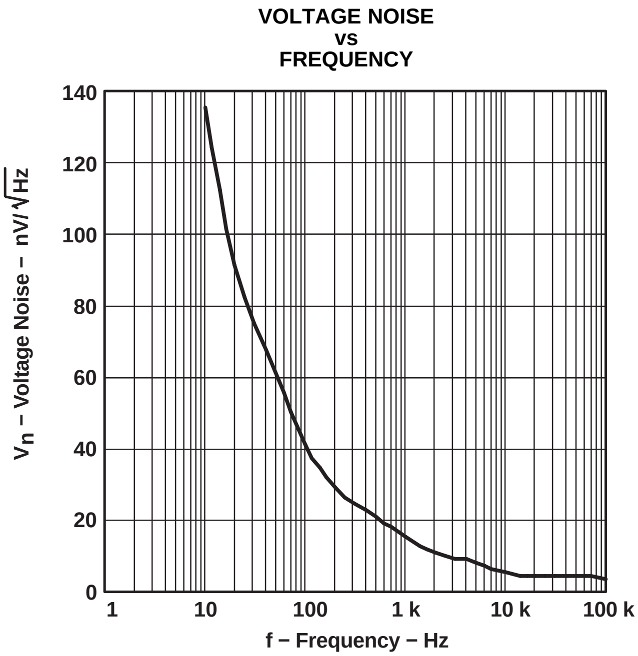


Figure 13.

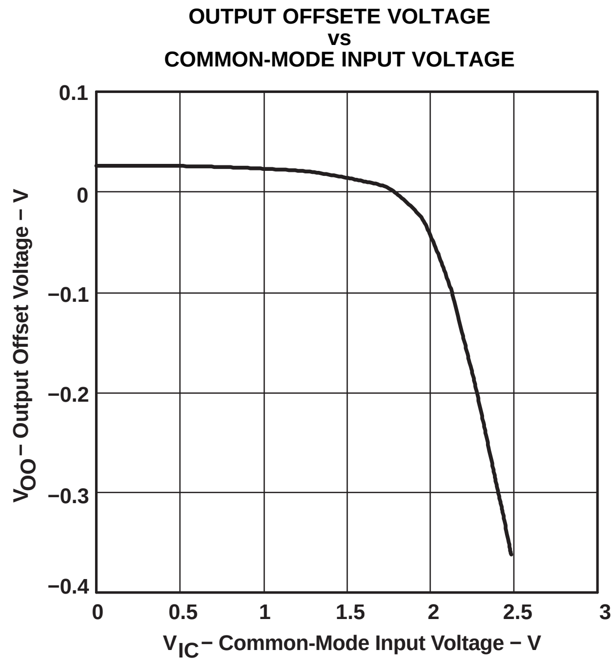


Figure 14.

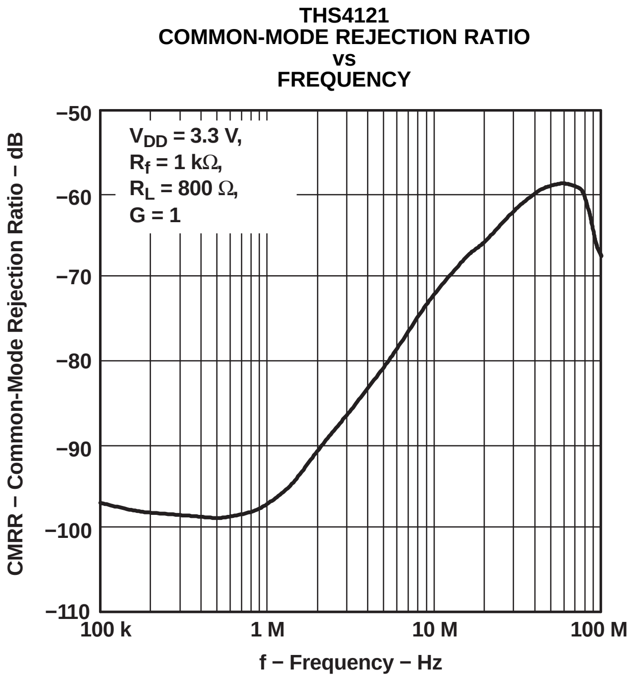


Figure 15.

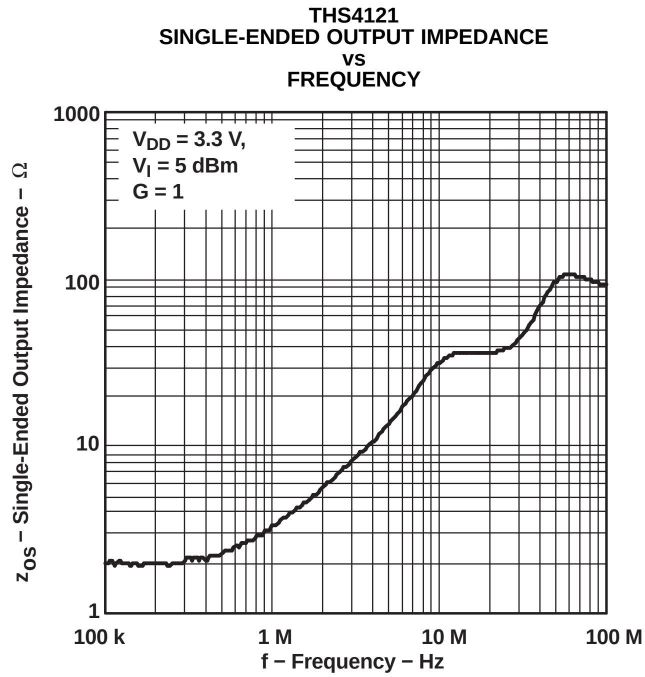


Figure 16.

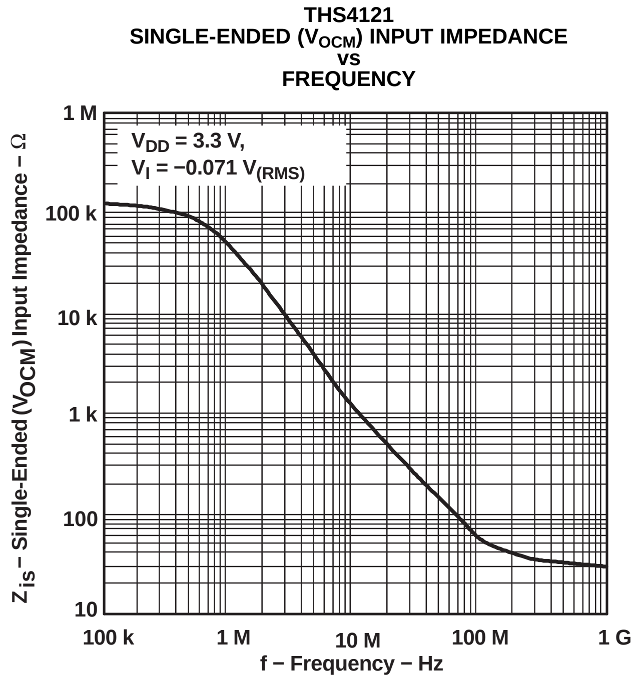

THS4121
SINGLE-ENDED (V_OCM) INPUT IMPEDANCE
vs
FREQUENCY
V_DD = 3.3 V,
V_I = −0.071 V_(RMS)
1 M
100 k
10 k
1 k
100
10
Z_is − Single-Ended (V_OCM) Input Impedance − Ω
100 k
1 M
10 M
100 M
1 G
f − Frequency − Hz

Figure 17.

APPLICATION INFORMATION

RESISTOR MATCHING

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it is set to the midrail voltage internally defined as:

$$\frac{\left(V_{DD}\right) + \left(V_{SS}\right)}{2} \tag{1}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input with the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1-µF capacitor on the V_{OCM} pin as a bypass capacitor. The following graph shows the simplified diagram of the THS412x.

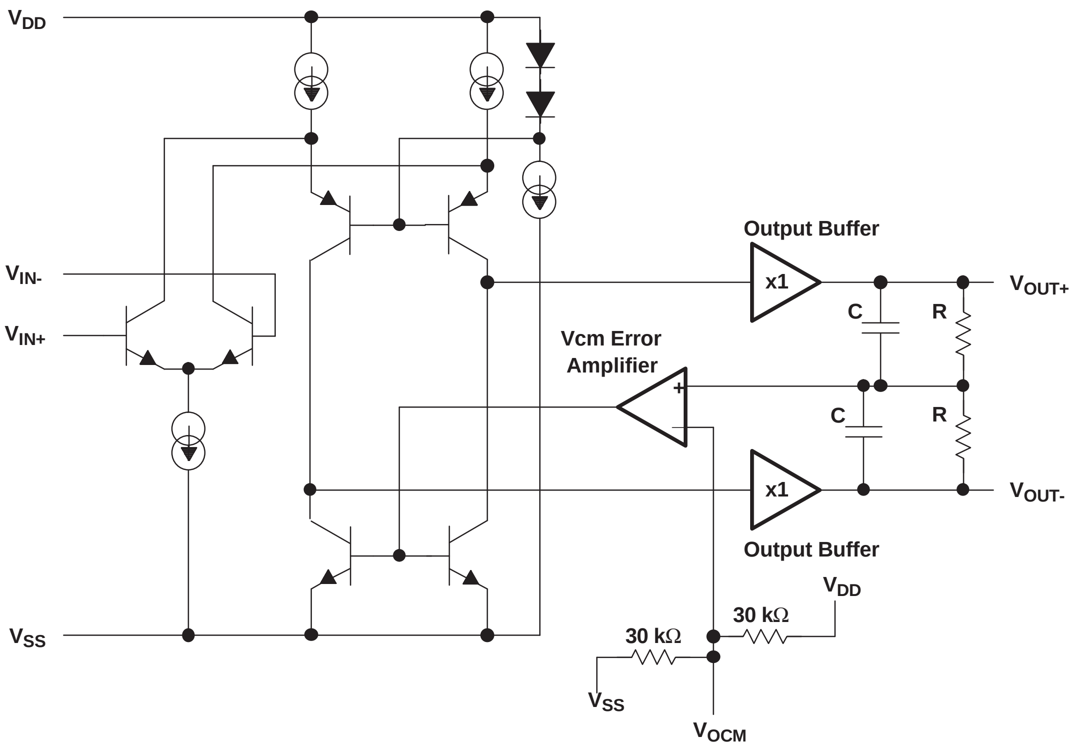


Figure 18. THS412x Simplified Diagram

APPLICATION INFORMATION (continued)

DATA CONVERTERS

Data converters are one of the most popular applications for the fully differential amplifiers.

Fully differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{DD}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

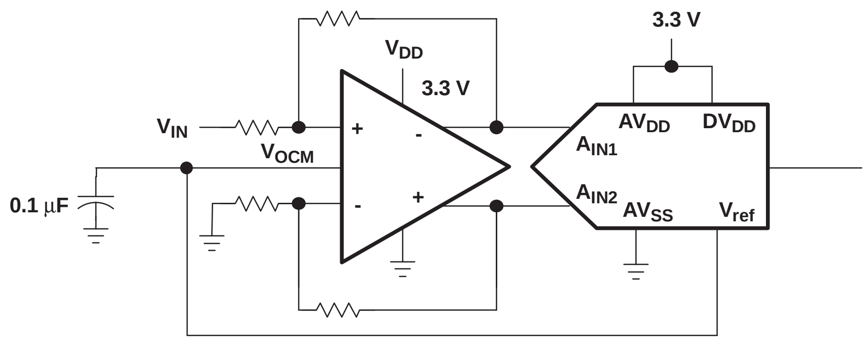


Figure 19. Differential Amplifier Using a Single Supply

Some single-supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the following circuit configuration is suggested to bring the common-mode input voltage within the specifications of the amplifier.

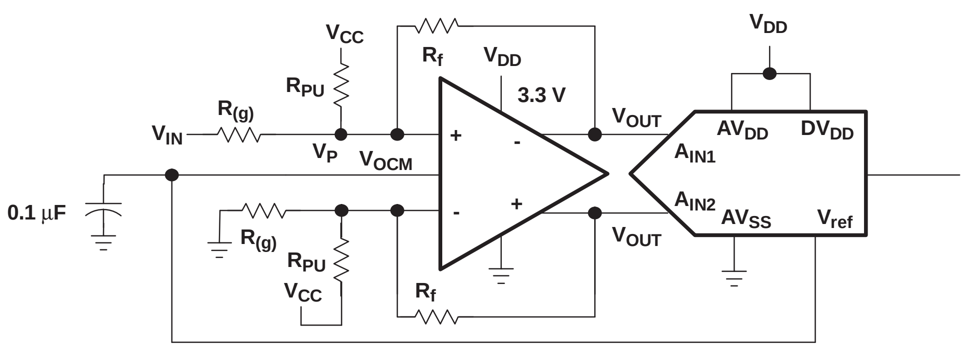


Figure 20. Circuit With Improved Common-Mode Input Voltage

The following equation is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{DD}}{\left(V_{IN} - V_P\right)\frac{1}{R_{(g)}} + \left(V_{OUT} - V_P\right)\frac{1}{R_f}} \quad (2)$$

APPLICATION INFORMATION (continued)

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS412x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 21. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

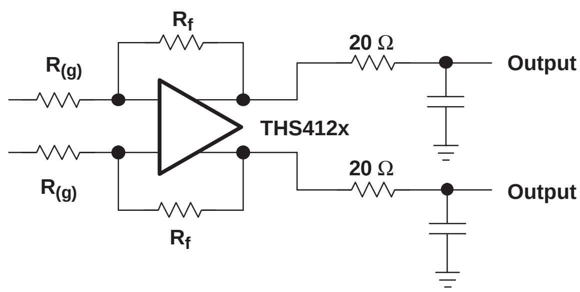


Figure 21. Driving a Capacitive Load

ACTIVE ANTIALIAS FILTERING

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. Figure 22 presents a method by which the noise may be filtered in the THS412x. Proper ground referencing should be considered.

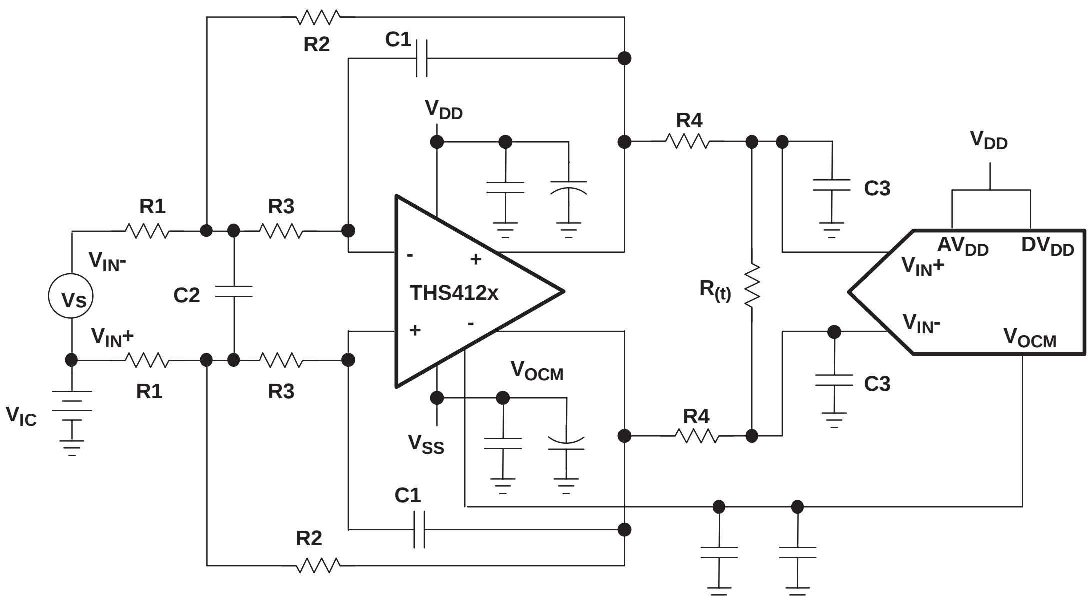


Figure 22. Antialias Filtering

APPLICATION INFORMATION (continued)

The transfer function for this filter circuit is:

$$H_d(f) = \left[\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right] \times \left[\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right] \quad \text{Where } K = \frac{R2}{R1} \tag{3}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \quad \text{and} \quad Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \tag{4}$$

K sets the pass-band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \quad \text{and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \tag{5}$$

Where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \quad \text{and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \tag{6}$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

PRINCIPLES OF OPERATION

THEORY OF OPERATION

The THS412x is a fully differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully differential amplifiers are *differential in/differential out*.

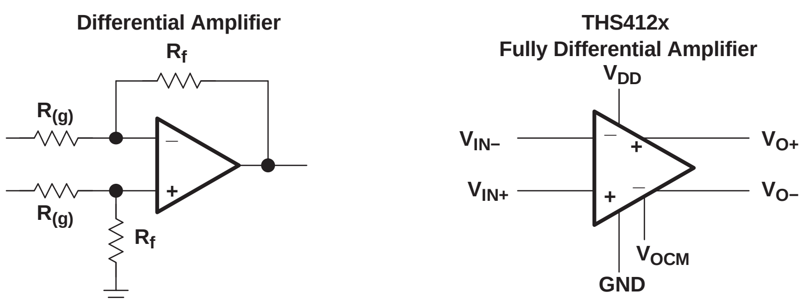


Figure 23. Differential Amplifier Versus a Fully Differential Amplifier

To understand the THS412x fully differential amplifiers, the definition for the pinouts of the amplifier are provided.

Input voltage definition $\quad V_{ID} = \left(V_{I+}\right) - \left(V_{I-}\right) \qquad V_{IC} = \frac{\left(V_{I+}\right) + \left(V_{I-}\right)}{2}$ (7)

Output voltage definition $\quad V_{OD} = \left(V_{O+}\right) - \left(V_{O-}\right) \qquad V_{OC} = \frac{\left(V_{O+}\right) + \left(V_{O-}\right)}{2}$ (8)

Transfer function $\quad V_{OD} = V_{ID} \times A_{(f)}$ (9)

Output common−mode voltage V_{OC} (10)

PRINCIPLES OF OPERATION (continued)

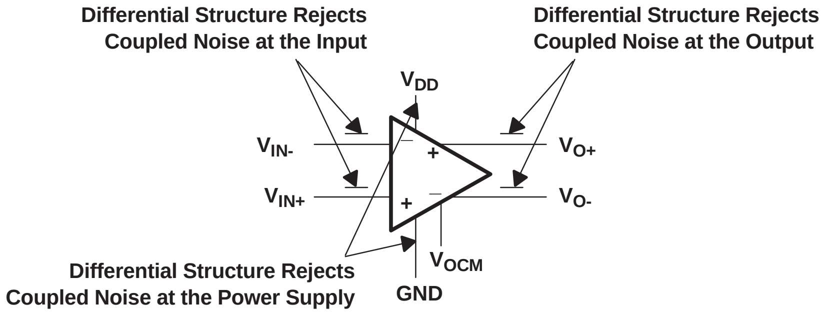


Figure 24. Definition of the Fully Differential Amplifier

The following schematics depict the differences between the operation of the THS412x, fully differential amplifier, in two different modes. Fully differential amplifiers can work with differential input or can be implemented as single in/differential out.

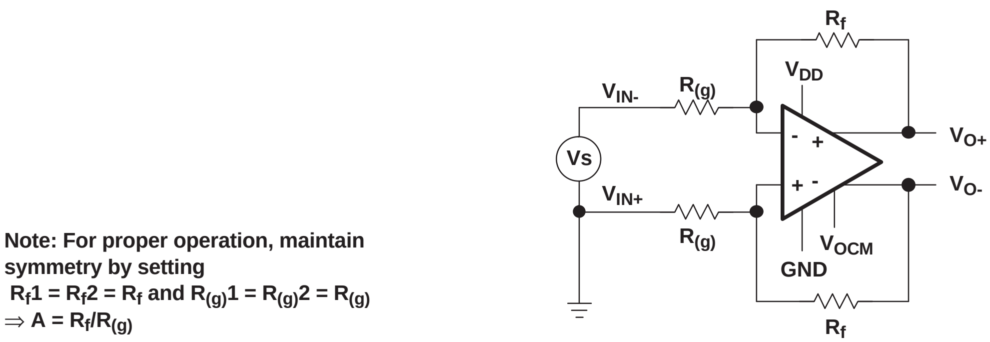
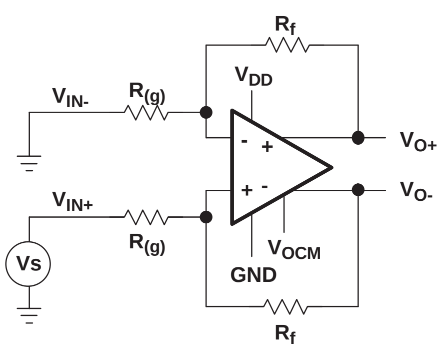


Figure 25. Amplifying Differential Signals



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	150	150

Figure 26. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I \quad (11)$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I \quad (12)$$

PRINCIPLES OF OPERATION (continued)

Fully differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it is not practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully differential amplifier. The final result indicates twice as much dynamic range. Figure 27 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS412x fully differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

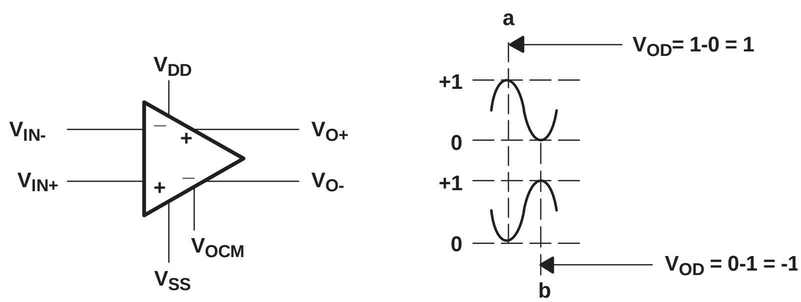


Figure 27. Fully Differential Amplifier With Two 1-V_{PP} Signals

CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high-frequency performance of the THS412x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS412x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes - It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling - Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch (2,54 mm) between the device power terminals and the ceramic capacitors.
- Sockets - Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements - Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components - Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

POWER-DOWN MODE

The THS4120 features a power-down pin ($\overline{PD}$) which lowers the quiescent current from 11 mA down to 120 µA, ideal for reducing system power. The power-down pin of the amplifier must be pulled high via a 10-kΩ pullup resistor between the $\overline{PD}$ pin and the positive supply (see Figure 28) in the absence of an applied voltage, putting

PRINCIPLES OF OPERATION (continued)

the amplifier in the power-on mode of operation. To turn off (disable) the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail or ground. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. The power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The enable time delay is in the order of microseconds due to the amplifier moving in and out of the linear mode of operation.

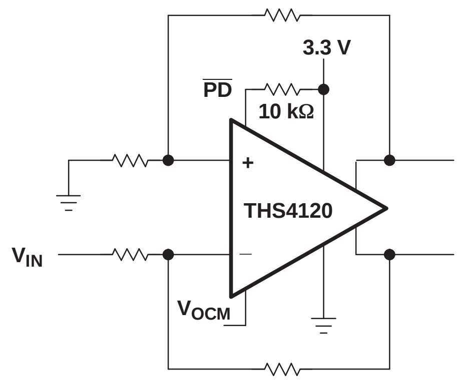


Figure 28.

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed-loop output impedance is shown in Figure 29.

PRINCIPLES OF OPERATION (continued)

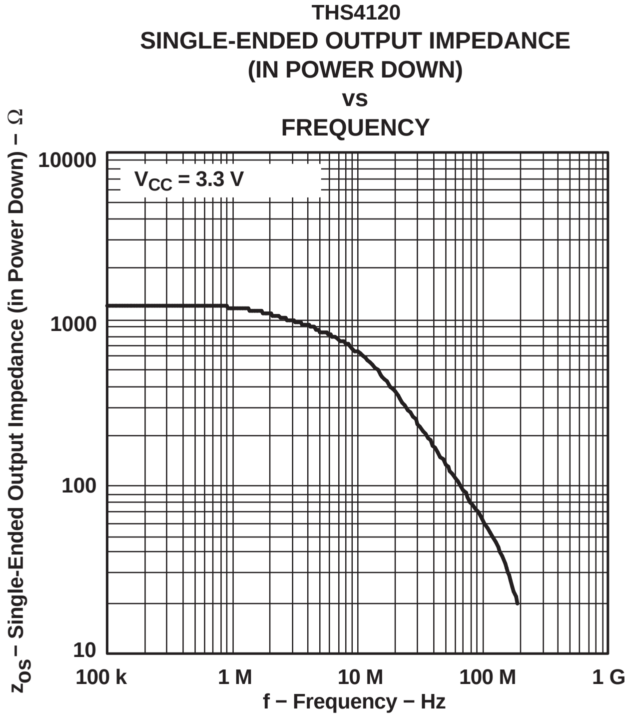


Figure 29.

PRINCIPLES OF OPERATION (continued)

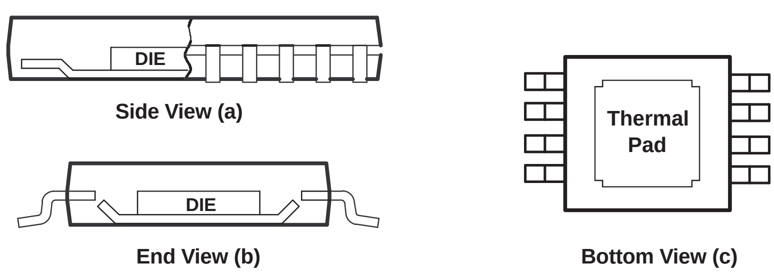
GENERAL PowerPAD DESIGN CONSIDERATIONS (APPLICABLE TO DIFFERENTIAL AMPLIFIER FAMILY)

The THS412x is available packaged in a thermally enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe on which the die is mounted [see Figure 30(a) and Figure 30(b)]. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package [see Figure 30(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package* (SLMA002). This document can be found at the TI Web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 30. Views of Thermally Enhanced DGN Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4120CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4120C	Samples
THS4120CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ARL	Samples
THS4120CDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ARL	Samples
THS4120CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ARL	Samples
THS4120CDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ARL	Samples
THS4120ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4120I	Samples
THS4120IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4120I	Samples
THS4120IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARN	Samples
THS4120IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARN	Samples
THS4120IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARM	Samples
THS4120IDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARM	Samples
THS4120IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARM	Samples
THS4120IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4120I	Samples
THS4121CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4121C	Samples
THS4121CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATO	Samples
THS4121CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATO	Samples
THS4121CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ASB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4121CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ASB	Samples
THS4121ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4121I	Samples
THS4121IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4121I	Samples
THS4121IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ASN	Samples
THS4121IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ASN	Samples
THS4121IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ASN	Samples
THS4121IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ASC	Samples
THS4121IDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASC	Samples
THS4121IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ASC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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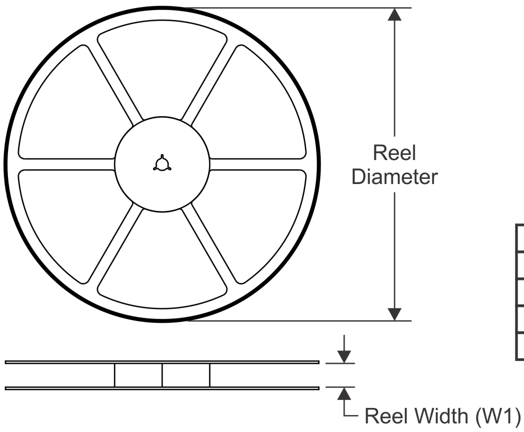
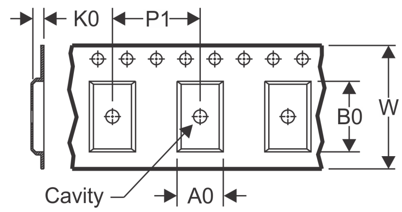
TAPE AND REEL INFORMATION

REEL DIMENSIONS

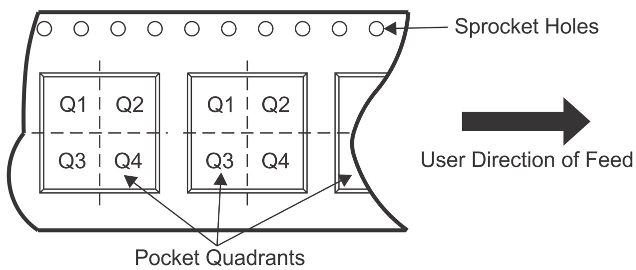


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

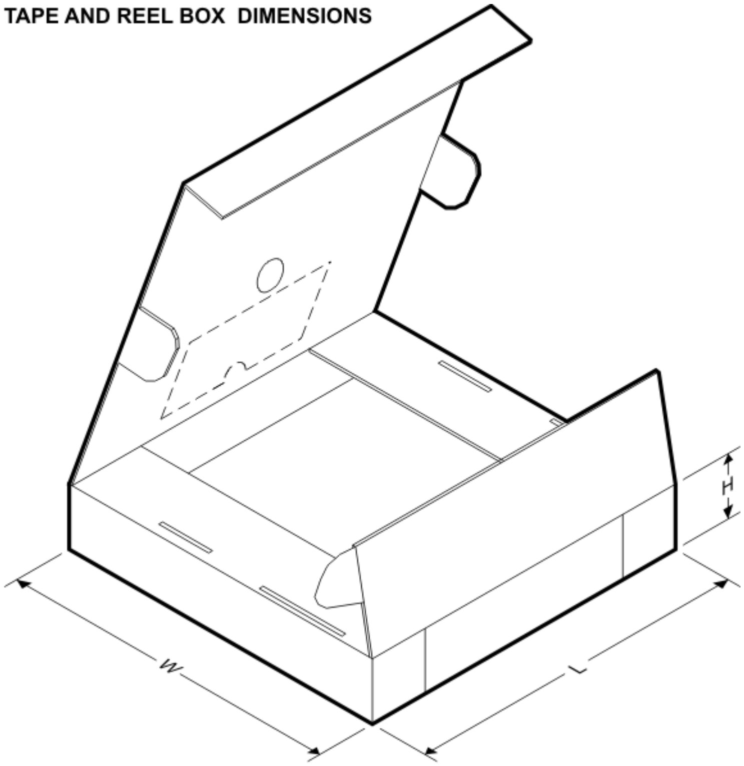
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4120CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4120IDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4120IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4121CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4121CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4121IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4121IDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

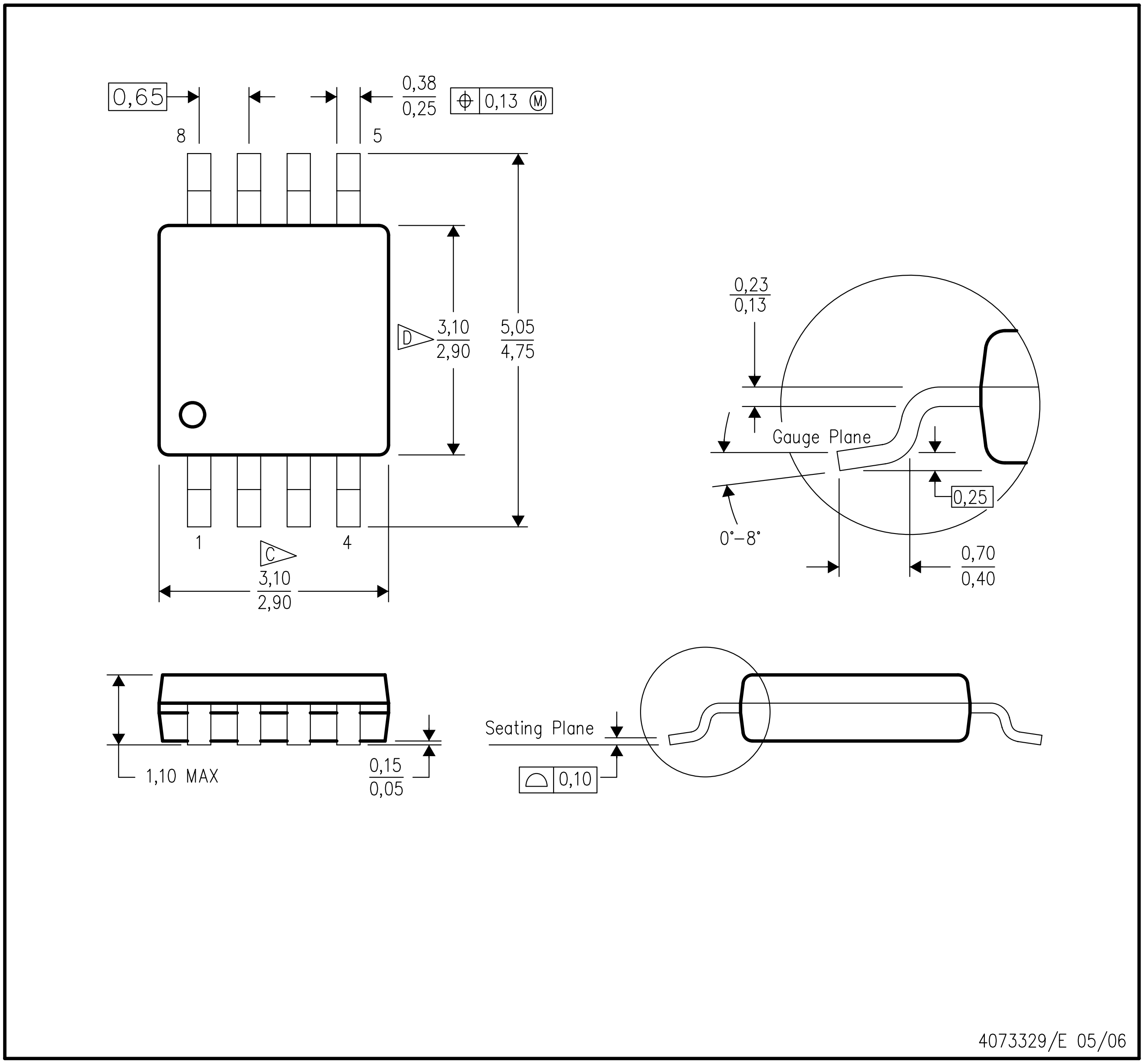
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

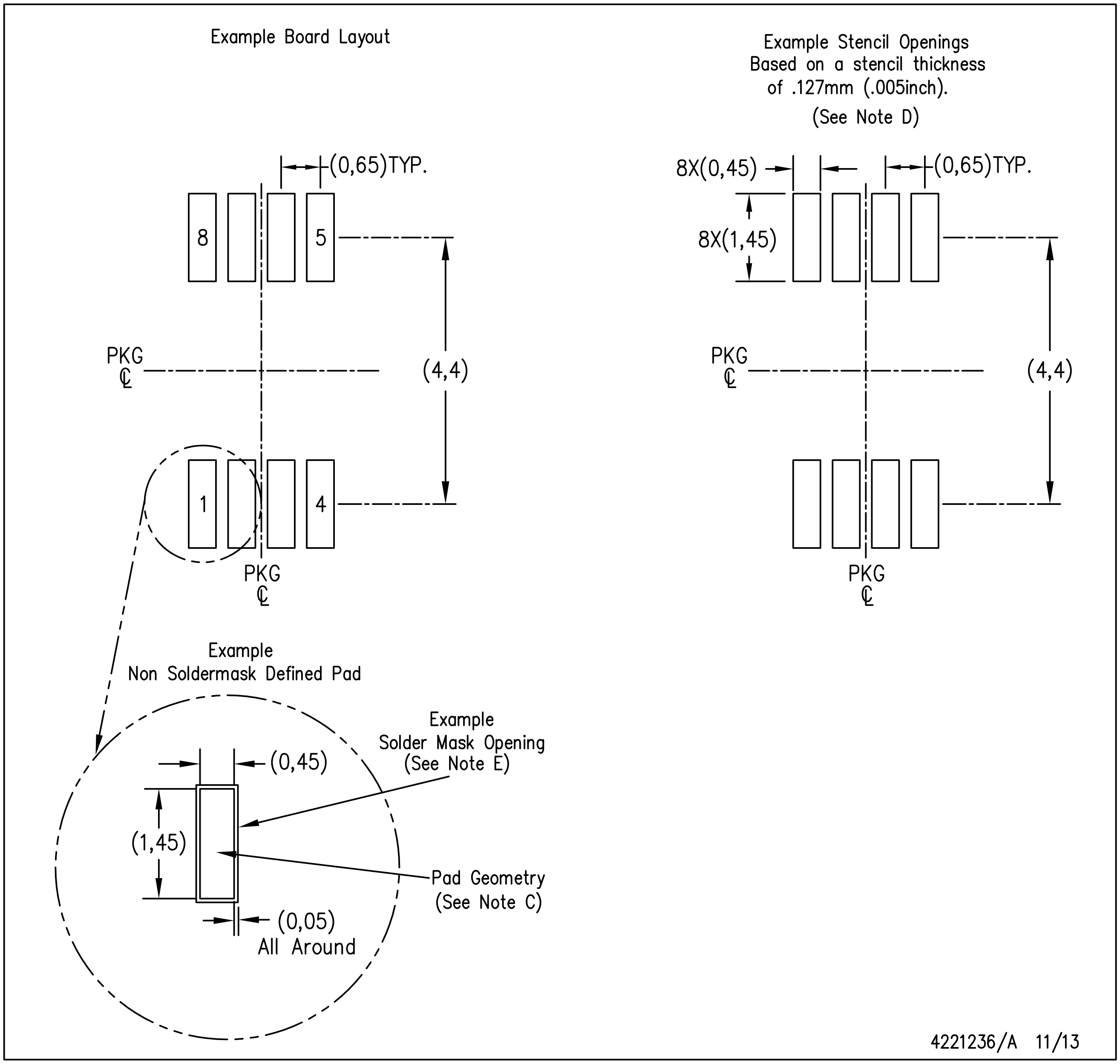
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4120CDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4120IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4120IDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4121CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4121CDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4121IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4121IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



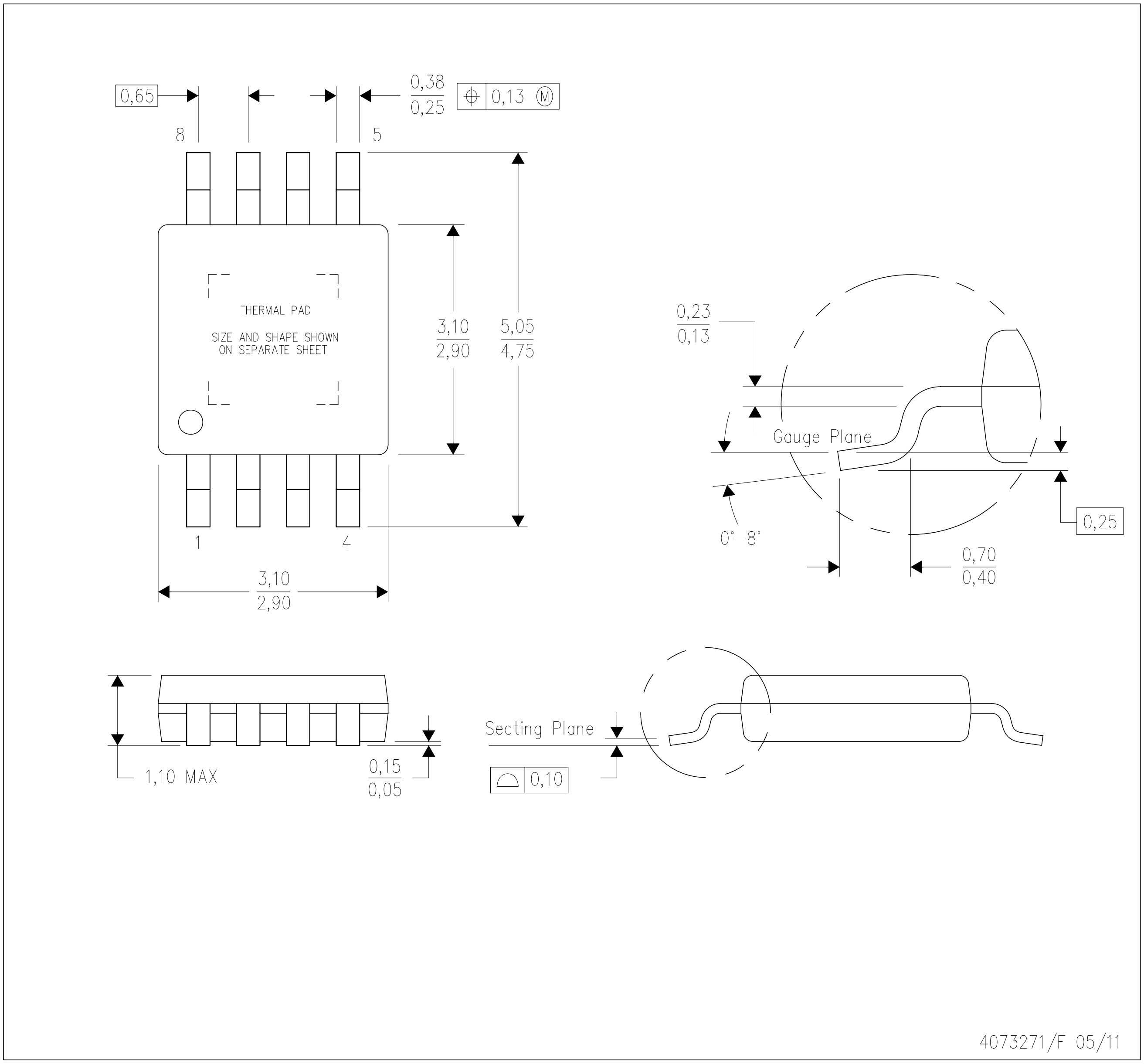
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

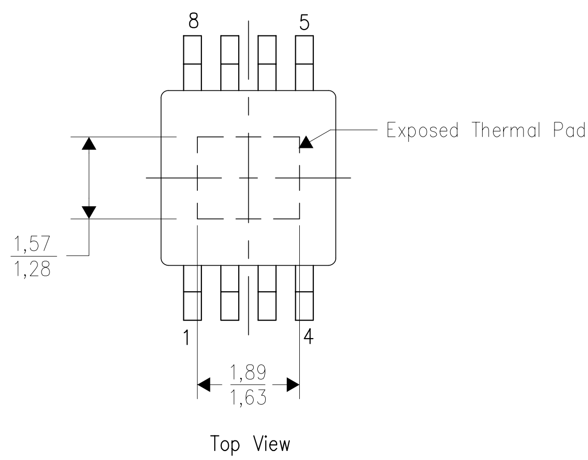
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



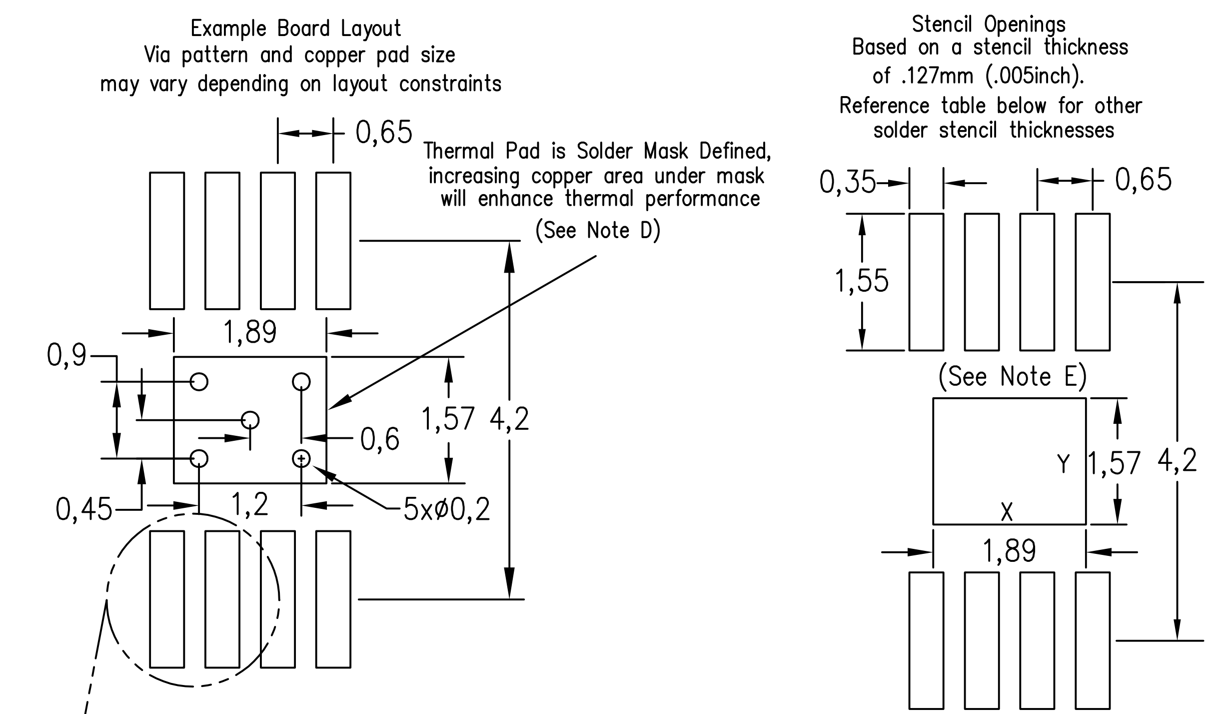
Exposed Thermal Pad Dimensions

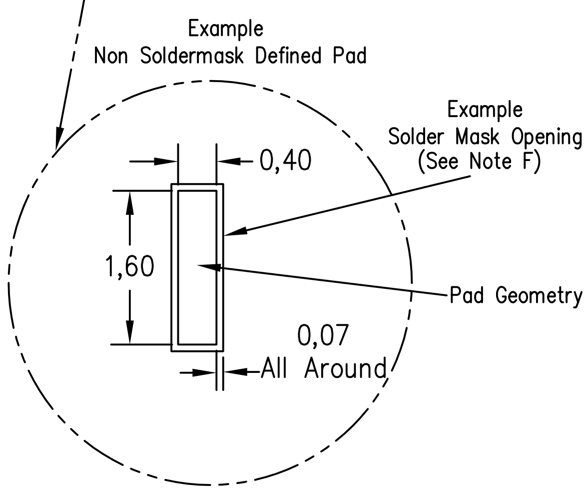
4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



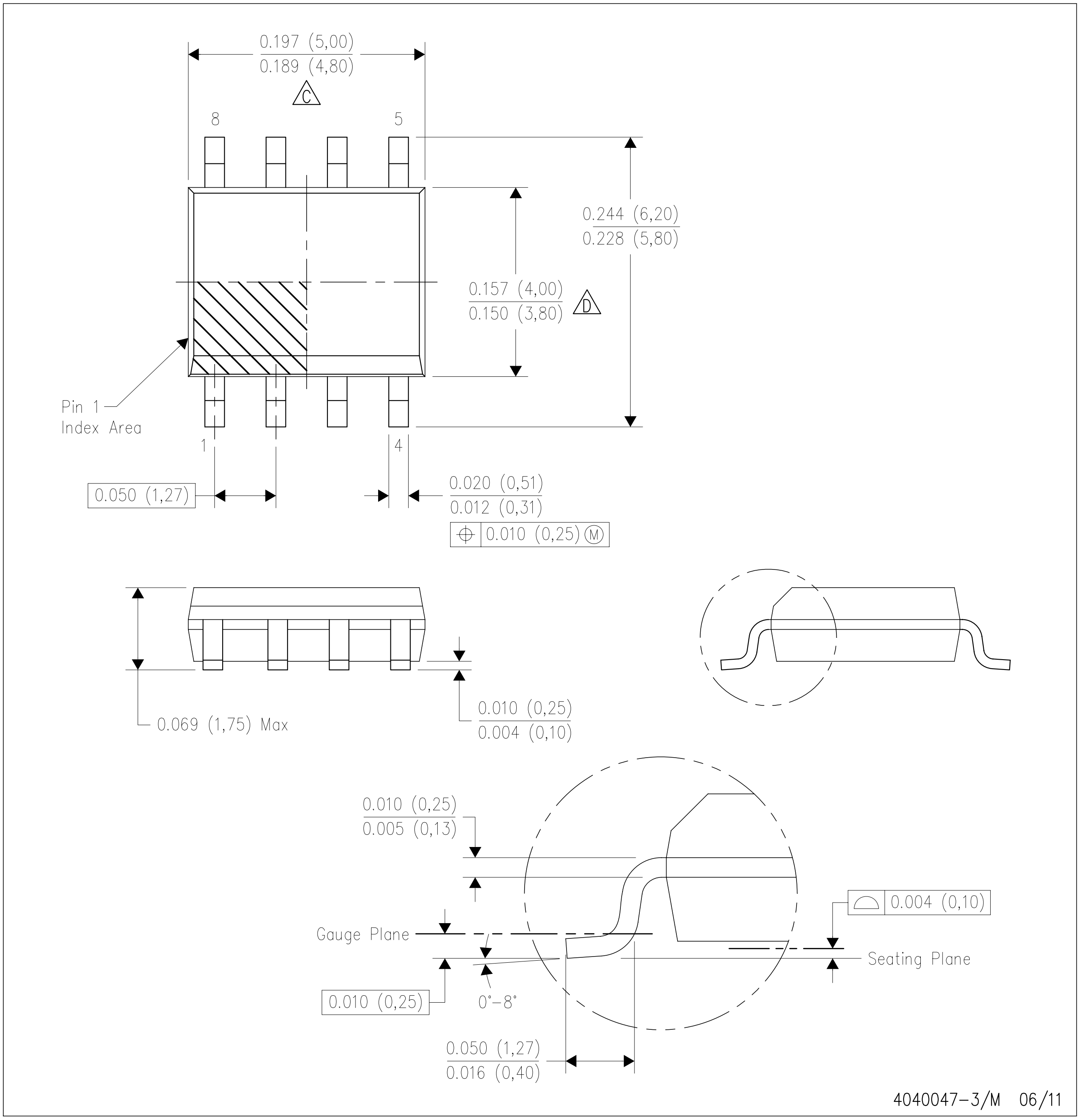


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/F 02/13

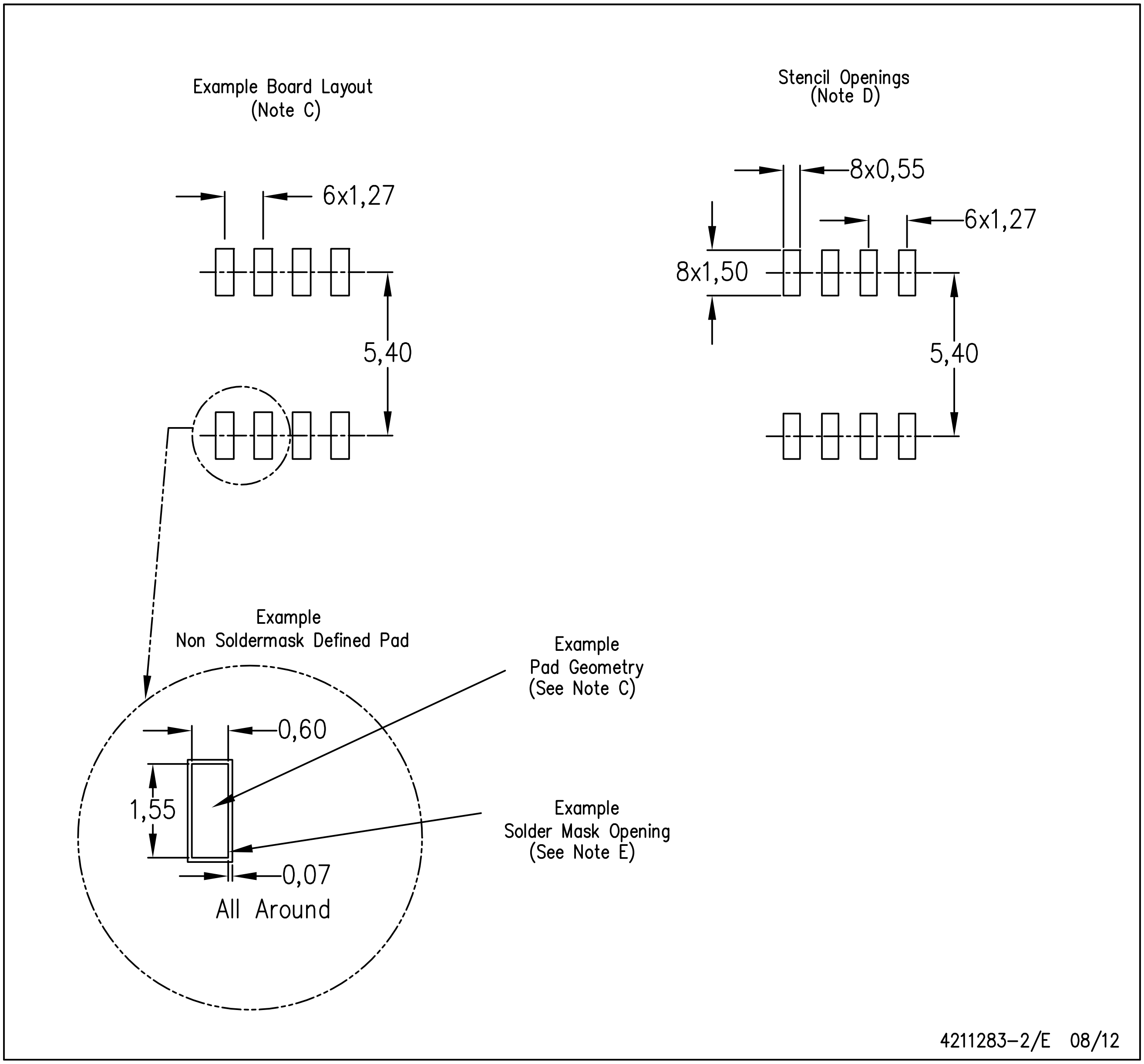
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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